

1. A circuit that allows a processor forming a part of a microcontroller to change its operating frequency, comprising:
- a clock generator generating a plurality of clock signals at a plurality of frequencies;
 - a first switch receiving the plurality of clock signals and selecting one of the clock signals as an output thereof to be the current clock according to a current speed select signal;
 - a current speed latch storing the current speed select signal;
 - a first phase shifter shifting the phase of the current clock to produce a phase shifted current clock;
 - a second switch receiving the plurality of clock signals and selecting one of the clock signals as an output thereof to be the new clock according to a new speed select signal;
 - a new speed register storing the new speed select signal;
- wherein, the new speed select signal is produced by the processor and stored in the new speed register;
- a second phase shifter shifting the phase of the new clock to produce a phase shifted new clock; and
- logic means, receiving the current clock, the phase shifted current clock, the new clock, the phase shifted new clock and a signal from the processor directing a speed change as inputs thereto, the logic means for producing a signal latching the new speed into the current speed latch at a point in time after the speed change signal when the current clock, phase shifted current clock, the new clock and the phase shifted new clock have the same state.
2. The apparatus according to claim 1, wherein the first and second phase shifter comprise a fixed delay circuit.

1 3. The apparatus according to claim 1, wherein the first and second phase
2 shifter comprise a fixed delay circuit producing a fixed delay of approximately 21
3 microseconds.

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5 4. The apparatus according to claim 1, wherein the logic means comprises a
6 logic NOR gate.

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8 5. The apparatus according to claim 1, wherein the speed change signal
9 comprises an I/O write signal.

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11 6. The apparatus according to claim 1, wherein the plurality of clock signals are
12 generated by dividing a master clock using a series of flip-flops.

1 7. A circuit that allows a processor forming a part of a microcontroller to
2 change its operating frequency, comprising:

3 a clock generator generating a plurality of clock signals at a plurality of
4 frequencies;

5 a first switch receiving the plurality of clock signals and selecting one of the
6 clock signals as an output thereof to be the current clock according to a current
7 speed select signal;

8 a current speed latch storing the current speed select signal;

9 a first phase shifter shifting the phase of the current clock to produce a
10 phase shifted current clock;

11 a second switch receiving the plurality of clock signals and selecting one
12 of the clock signals as an output thereof to be the new clock according to a new
13 speed select signal;

14 a new speed register storing the new speed select signal;

15 wherein, the new speed select signal is produced by the processor and
16 stored in the new speed register;

17 a second phase shifter shifting the phase of the new clock to produce a
18 phase shifted new clock;

19 logic means, receiving the current clock, the phase shifted current clock, the
20 new clock, the phase shifted new clock and a signal from the processor directing
21 a speed change as inputs thereto; and

22 the logic means producing a latching signal latching the new speed into the
23 current speed latch at a point in time after the speed change signal when the
24 current clock has the same state as the new clock, and when the phase shifted
25 current clock has the same state as the phase shifted new clock.

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27 8. The apparatus according to claim 7, wherein the first and second phase
28 shifter comprise a fixed delay circuit.

1 9. The apparatus according to claim 7, wherein the first and second phase
2 shifter comprise a fixed delay circuit producing a fixed delay of approximately 21
3 microseconds.

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5 10. The apparatus according to claim 7, wherein the logic means comprises a
6 logic NOR gate, and wherein the logic means for producing a signal latching the
7 new speed into the current speed latch at a point in time after the speed change
8 signal when the current clock has the same state as the new clock, the phase
9 shifted current clock and the phase shifted new clock.

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11 11. The apparatus according to claim 7, wherein the logic means comprises a
12 first EXOR gate receiving the current clock and the new clock and a second EXOR
13 gate receiving the phase shifted current clock and the phase shifted new clock, and
14 wherein the first and second EXOR gates have outputs connected to two inputs of
15 a NOR gate with the speed change signal connected to a third input of the NOR
16 gate and with an output of the NOR gate producing the latching signal.

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18 12. The apparatus according to claim 7, wherein the logic means comprises a
19 first NAND gate receiving the current clock and the new clock and a second NAND
20 gate receiving the phase shifted current clock and the phase shifted new clock, and
21 wherein the first and second NAND gates have outputs connected to two inputs of
22 a NOR gate with the speed change signal connected to a third input of the NOR
23 gate and with an output of the NOR gate producing the latching signal.

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25 13. The apparatus according to claim 7, wherein the plurality of clock signals are
26 generated by dividing a master clock using a series of flip-flops.

1 14. A circuit that allows a processor forming a part of a microcontroller to
2 change its operating frequency, comprising:

3 a master clock generating a master clock signal;

4 a clock generator generating a plurality of clock signals from the master
5 clock signal at a plurality of frequencies by dividing the master clock signal using
6 a plurality of series connected flip flops;

7 a first switch receiving the plurality of clock signals and selecting one of the
8 clock signals as an output thereof to be the current clock according to a current
9 speed select signal;

10 a current speed latch storing the current speed select signal;

11 a first phase shifter shifting the phase of the current clock to produce a
12 phase shifted current clock by delaying the current clock by a fixed delay;

13 a second switch receiving the plurality of clock signals and selecting one
14 of the clock signals as an output thereof to be the new clock according to a new
15 speed select signal;

16 a new speed register storing the new speed select signal;

17 wherein, the new speed select signal is produced by the processor and
18 stored in the new speed register;

19 a second phase shifter shifting the phase of the new clock to produce a
20 phase shifted new clock by delaying the new clock by a fixed delay; and

21 a logic NOR gate, receiving as inputs the current clock, the phase shifted
22 current clock, the new clock, the phase shifted new clock and a signal from the
23 processor directing a speed change as inputs thereto, the NOR gate producing a
24 signal latching the new speed into the current speed latch at a point in time when
25 speed change signal, the current clock, phase shifted current clock, the new clock
26 and the phase shifted new clock have the same state.

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28 15. The apparatus according to claim 1, wherein the first and second phase
29 shifter comprise a fixed delay circuit producing a fixed delay of approximately 21
30 microseconds.

1 16. A method for a processor forming a part of a microcontroller to change its
2 clock frequency, comprising:
3 at the processor, receiving a clock signal;
4 determining that the clock frequency is to be changed under program
5 control;
6 storing a new clock frequency signal in a new speed register;
7 issuing an I/O write command indicating that the clock frequency is to
8 change;
9 in a logic circuit, examining a current clock signal, a new clock signal, a
10 phase shifted current clock signal and a phase shifted new clock signal;
11 when the current clock signal, the new clock signal, the phase shifted
12 current clock signal and the phase shifted new clock signal reach predetermined
13 states, latching the new clock frequency signal into a current clock speed latch;
14 and
15 at a switch, receiving an output from the current clock speed latch and
16 changing a switch setting in response thereto, the switch setting determining the
17 speed of the clock signal.
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19 17. The method according to claim 16, further comprising providing the new
20 clock signal and the phase shifted new clock signal to the logic circuit through a
21 switch.
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23 18. The method according to claim 16, wherein the switch receives a plurality
24 of clock signals produced from a master clock signal.
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26 19. The apparatus according to claim 16, wherein the phase shifted current
27 clock and the phase shifted new clock are delayed versions of the current clock
28 and the new clock respectively, with the delay being a fixed constant delay.
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1 20. The method according to claim 16, wherein the logic circuit examines the
2 current clock signal, the new clock signal, the phase shifted current clock signal
3 and the phase shifted new clock signal to determine that at least the current clock
4 signal has the same state as the new clock signal and the phase shifted current
5 clock signal has the same state as the phase shifted new clock signal.
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